Claims

1. A method for transferring analog image signals of a CCD camera line by line into the memory (RAM) of an electronic unit working with a digital signal processor (DSP) for image processing, in which the image data is digitized by means of a video processor (VIP), comprising the processing steps of

a) tripping of an interrupt at the DSP by an image synchronizing signal,

b) initiating an interrupt routine by the DSP,

c) putting out an interrupt release signal by the DSP,

d) switching the system timing of the DSP to the timing of the VIP, the interrupt release signal issued becomes effective at a logic unit serving to switch over the clock pulse frequency,

e) issuing a RAM address to generate a chip-select signal to address a memory address in the address space of the VIP,

f) generating and issuing a READ signal by the DSP,

g) incrementing the last issued RAM address by the DSP, in each case after transmission of image data characterizing one pixel of the image into the RAM,

the interrupt release signal becoming effective at the logic unit for switching over the timing as soon as the system timing of the DSP, the system timing of the VIP as well as the image pixel timing of the VIP have the same timing condition, and the process steps c) to g) being carried out in the course of processing the interrupt routine called up in process step b), and the READ, signal issued by the DSP in accordance with process step f), acting as a write signal at the RAM as a result of an inversion, so that, as a result of the READ signal, the image data queued at the VIP is read over the data bus, and written directly into the RAM, which is acted upon with the WRITE-signal.

2. The method of claim 1, wherein the DSP, within the line gating gap, continues to carry out further processing at the timing of the VIP, while the DSP, after reading in one of the half-images transferred from the CCD camera according to the line jump method, is switched back to the original system timing by resetting the interrupt release signal.

3. Circuit arrangement for transferring analog image signals of a CCD camera into a memory (RAM) (70) of an electronic unit for image processing, working with a digital signal processor (DSP) (50) which, in addition to the DSP (50) and the RAM (70), has at least one video processor (VIP) (60) to digitize the image data, a write-read control (80) for the RAM (70), a first clock pulse supplier for the DSP (50), a second clock pulse supplier with a clock pulse rate, which is lower than the clock pulse supplier, for the VIP (60) and the DSP (50), a data bus (90) as well as a logic unit (100) for changing over the timing, to which the clock pulse signals of the first and second clock pulse supplier as well as the image pixel timing of the VIP (60) and an interrupt release signal of the DSP (50) are supplied, so that the DSP (50) is coupled over the logic unit (100) alternately with the first or the second clock pulse supplier, while the logic unit (100), in each case, at the same level position of the clock pulse signals supplied to it, takes over the actual level of the interrupt release signal, and corresponding to this level, switches through the clock pulse signal of the first or second clock pulse supplier for clocking the DSP (50), wherein, during the transfer of image data to the RAM (70), the clock pulse signal of the clock pulse supplier clocking the VIP (60) is also switched through at the lower clock pulse rate to the DSP (50) and, as a result of a prior inversion in the write-read control (80), act as WRITE signals at the RAM (70).

4. The circuit arrangement of claim 3, wherein the clock pulse is supplied to the DSP (50) is over the output (14) of a clock pulse separating filter (1) of the logic unit (100) for switching the timing, to which the first clock pulse signal is supplied over a first input (11) and the second clock pulse signal is supplied over a

second input (12), and which is connected over a third input (13) to the output (24) of a flip-flop (2), which is wired at its D-input (21) with the interrupt release signal emitted by the DSP (50) after an interrupt, tripped by the image synchronization signal and connected at its clock pulse input (22) with the output (34) of a gate (3), which AND connects the clock pulse signals of the first and second clock pulse suppliers as well as the image pixel timing of the VIP (60) with one another.

5. The circuit of claim 4, wherein the setting of the flip-flop (2) and the therewith associated clock pulse switching over of the DSP (50) to the lower timing of the VIP (60) is accomplished by means of the transfer, flank-controlled by means of the clock pulse input (22), of the interrupt release signal, which is switched to the D-input (21) of the flip-flop (2) and is put out by the DSP (50) after an interrupt tripped by the image synchronizing signal,

6. The circuit of claims 4 or 5, wherein, in the input area (15, 16) of the clock pulse separating filter (1), a gate circuit is provided, by means of which an AND linkage of the clock pulse signal for the VIP (60) with the output signal of the flip-flop (2) is brought about and an AND linkage of the higher timing, clocking the DSP (50) during actual processing of the image, with the inverted output signal of the flip-flop (2) is brought about and that, in the output area (17, 18) of the clock pulse separating filter (1), a gate circuit for the OR connection of the output signals of the gate circuit, disposed in the input area (15, 16) of the clock pulse separating filter (1) is provided.

7. The circuit of claim 6, wherein the gate circuit in the input area (15, 16) of the clock pulse separating filter (1) is constructed so that the clock pulse signals, supplied to the clock pulse separating filter are inverted before their AND linkage with the output signal and/or the inverted output signal of the flip-flop (2) and wherein the gate circuit, provided for the OR linkage in the output area (17, 18) of the clock pulse separating filter (1) is constructed as a NOR-gate (17) with an inverter (18) connected in series.

8. The circuit of claims 4 to 7, wherein, to accelerate the clock pulse signal originally clocking the DSP (50), the RESET input (23) of the flip-flop (2) is connected with the D input (21) of the latter, an inverter (40) being disposed in the connection between the D input (21) and the RESET input (23) for the case that the level, tripping the flip-flop (2), is opposed to that output level of the flip-flop (2), through which the temporary switching over to the second timing takes place.